What Is Claimed Is:

1. An apparatus that facilitates implementing a memory mechanism within an asynchronous switch fabric, comprising:

a memory device, wherein the memory device has other than first-in, first-out semantics including one of a random access memory and a stack;

a data destination horn, for routing data from a trunk line to a plurality of destinations, wherein the memory device is a destination of the plurality of destinations; and

a data source funnel, for routing data from a plurality of sources into the trunk line, wherein the memory device is a source of the plurality of sources.

2. The apparatus of claim 1, further comprising:

an asynchronous control structure coupled to the data destination horn, that is configured to control propagation of data through the data destination horn;

wherein the asynchronous control structure is additionally coupled to the data source funnel, and is additionally configured to control propagation of data through the data source funnel;

wherein the asynchronous control structure uses a destination address associated with the data destination horn for the memory device to control propagation of data to the memory device; and

wherein the asynchronous control structure uses the destination address for the memory device to control propagation of data from the memory device.

3. The apparatus of claim 2, wherein a read address for the memory device is shared as a write address of the data destination horn for the memory

device, so that an order of memory operations for the memory device is identical to an instruction order for the memory device.

4. The apparatus of claim 3, wherein a literal value associated with an instruction for the memory device can specify one of a write operation and a read operation.

5. The apparatus of claim 4, further comprising a first-in, first-out storage structure interposed between the memory device and the data source funnel so that data delivered from the memory device during the read operation will be available to the data source funnel in a same order as delivered from the memory device.

6. The apparatus of claim 1, further comprising:

an asynchronous control structure coupled to the data destination horn, that is configured to control propagation of data through the data destination horn;

wherein the asynchronous control structure is additionally coupled to the data source funnel, and is additionally configured to control propagation of data through the data source funnel;

wherein the asynchronous control structure uses a source address associated with the data source funnel for the memory device to control propagation of data to the memory device; and

wherein the asynchronous control structure uses the source address for the memory device to control propagation of data from the memory device.

7. The apparatus of claim 6, wherein a write address for the memory device is shared as a read address of the data source funnel for the memory device,

so that an order of memory operations for the memory device is identical to an instruction order for the memory device.

8. The apparatus of claim 7, wherein a literal value associated with an instruction for the memory device can specify one of a write operation and a read operation.

9. The apparatus of claim 8, further comprising a first-in, first-out storage structure interposed between the data destination horn and the memory device so that data delivered from the data destination horn during the write operation will be available to the memory device in a same order as delivered from the data destination horn.

10. The apparatus of claim 1, wherein the apparatus converts the memory device with other than first-in, first-out semantics to into a dual-port device with first-in, first-out semantics, wherein read/write order hazards are avoided by assigning read and write control to a single port of the dual-port device.

11. A computing system that facilitates implementing a memory mechanism within an asynchronous switch fabric, comprising:

a memory device, wherein the memory device has other than first-in, first-out semantics including one of a random access memory and a stack;

a data destination horn, for routing data from a trunk line to a plurality of destinations, wherein the memory device is a destination of the plurality of destinations; and

a data source funnel, for routing data from a plurality of sources into the trunk line, wherein the memory device is a source of the plurality of sources.

12. The computing system of claim 11, further comprising:

an asynchronous control structure coupled to the data destination horn, that is configured to control propagation of data through the data destination horn;

wherein the asynchronous control structure is additionally coupled to the data source funnel, and is additionally configured to control propagation of data through the data source funnel;

wherein the asynchronous control structure uses a destination address associated with the data destination horn for the memory device to control propagation of data to the memory device; and

wherein the asynchronous control structure uses the destination address for the memory device to control propagation of data from the memory device.

13. The computing system of claim 12, wherein a read address for the memory device is shared as a write address of the data destination horn for the memory device, so that an order of memory operations for the memory device is identical to an instruction order for the memory device.

14. The computing system of claim 13, wherein a literal value associated with an instruction for the memory device can specify one of a write operation and a read operation.

15. The computing system of claim 14, further comprising a first-in, first-out storage structure interposed between the memory device and the data source funnel so that data delivered from the memory device during the read

operation will be available to the data source funnel in a same order as delivered from the memory device.

16. The computing system of claim 11, further comprising:

an asynchronous control structure coupled to the data destination horn, that is configured to control propagation of data through the data destination horn;

wherein the asynchronous control structure is additionally coupled to the data source funnel, and is additionally configured to control propagation of data through the data source funnel;

wherein the asynchronous control structure uses a source address associated with the data source funnel for the memory device to control propagation of data to the memory device; and

wherein the asynchronous control structure uses the source address for the memory device to control propagation of data from the memory device.

17. The computing system of claim 16, wherein a write address for the memory device is shared as a read address of the data source funnel for the memory device, so that an order of memory operations for the memory device is identical to an instruction order for the memory device.

18. The computing system of claim 17, wherein a literal value associated with an instruction for the memory device can specify one of a write operation and a read operation.

19. The computing system of claim 18, further comprising a first-in, first-out storage structure interposed between the data destination horn and the memory device so that data delivered from the data destination horn during the

write operation will be available to the memory device in a same order as delivered from the data destination horn.

20. The apparatus of claim 11, wherein the apparatus converts the memory device with other than first-in, first-out semantics to into a dual-port device with first-in, first-out semantics, wherein read/write order hazards are avoided by assigning read and write control to a single port of the dual-port device.

21. A method for implementing a memory mechanism within an asynchronous switch fabric, wherein the memory mechanism is a memory device with other than first-in, first-out semantics including one of a random access memory and a stack, comprising:

accepting data from a trunk line to a data destination horn;

routing data to a plurality of destinations from the data destination horn, wherein the memory device is a destination of the plurality of destinations;

addressing the memory device using a destination address within an asynchronous control structure, wherein the destination address is used to store data in the memory device and to recover data from the memory device;

decoding an additional address bit to select one of a memory read and a memory write;

providing data to a first-in, first-out storage structure from the memory device;

receiving data from the first-in, first-out storage structure at a data source funnel; and

applying data from the data source funnel to the trunk line.

22. A method for implementing a memory mechanism within an asynchronous switch fabric, wherein the memory mechanism includes a memory device with other than first-in, first-out semantics, comprising:

accepting data from a trunk line to a data destination horn;

routing data to a plurality of destinations from the data destination horn, wherein a first-in, first-out storage structure is a destination of the plurality of destinations;

providing data to the memory device from the first-in, first-out storage structure;

addressing the memory device using a source address within an asynchronous control structure, wherein the source address is used to store data in the memory device and to recover data from the memory device;

decoding an additional address bit to select one of a memory read and a memory write;

receiving data from the memory device at a data source funnel; and

applying data from the data source funnel to the trunk line.